15:31:56 DEBUG src/lib/components/cu/cu.c:452: Running S1

15:31:56 DEBUG src/lib/components/cu/cu.c:132: Decoding opcode: 0xBF

15:31:56 WARN src/lib/components/cu/cu.c:422: Unhandled opcode: 0xBF

15:31:56 INFO src/main.c:46: Cycle time: 0.000020s => 50.000000 KHz

15:31:56 INFO src/main.c:24: Press enter to continue...

15:31:57 DEBUG src/lib/components/cu/cu.c:452: Running S0

15:31:57 INFO src/main.c:46: Cycle time: 0.000031s => 32.258065 KHz

15:31:57 INFO src/main.c:24: Press enter to continue...

15:31:58 DEBUG src/lib/components/cu/cu.c:452: Running S1

15:31:58 DEBUG src/lib/components/cu/cu.c:132: Decoding opcode: 0x70

15:31:58 INFO src/main.c:46: Cycle time: 0.000026s => 38.461538 KHz

15:31:58 INFO src/main.c:24: Press enter to continue...

15:32:06 DEBUG src/lib/components/cu/cu.c:452: Running S16

15:32:06 INFO src/main.c:46: Cycle time: 0.000026s => 38.461538 KHz

15:32:06 INFO src/main.c:24: Press enter to continue...

15:32:07 DEBUG src/lib/components/cu/cu.c:452: Running S17

15:32:07 INFO src/main.c:46: Cycle time: 0.000023s => 43.478261 KHz

15:32:07 INFO src/main.c:24: Press enter to continue...

15:32:09 DEBUG src/lib/components/cu/cu.c:452: Running S18

15:32:09 INFO src/main.c:46: Cycle time: 0.000021s => 47.619048 KHz

15:32:09 INFO src/main.c:24: Press enter to continue...

15:32:10 DEBUG src/lib/components/cu/cu.c:452: Running S4

15:32:10 INFO src/main.c:46: Cycle time: 0.000060s => 16.666667 KHz

15:32:10 INFO src/main.c:24: Press enter to continue...

15:32:14 DEBUG src/lib/components/cu/cu.c:452: Running S0

15:32:14 INFO src/main.c:46: Cycle time: 0.000021s => 47.619048 KHz

15:32:14 INFO src/main.c:24: Press enter to continue...

**Estado S0**: Se coge la instrucción de memoria y se guarda en el RI.

**Estado S1**: Se decodifica la instrucción. En este caso al RI = 0x70, se deduce que se está haciendo un LDA dir:

|  |  |
| --- | --- |
| **70** | **LDA dir: AC 🡨 (dir)** |
| S0 | RI 🡨 (PC), PC + 1 |
| S1 | DECODE |
| S16 | H 🡨 (PC), PC + 1 |
| S17 | L 🡨 (PC), PC + 1 |
| S18 | 2OP 🡨 PC + 1 |
| S4 | AC 🡨 2OP |

El decode sabe que los siguientes van a ser: S16 🡪 S17 🡪 S18 🡪 S4.

En los siguientes ciclos de reloj se ejecutan dichos estados. Al no existir un estado posterior al S4, se ejecuta el estado S0, y se vuelve a iniciar el procedimiento.

Nota: si el decode no encuentra el opcode, se ejecuta el estado S0. (En el ejemplo “Unhandled opcode: 0xBF”)